PVP 20

Code: 20EC6401

II B.Tech - II Semester – Regular Examinations – MAY 2023

DIGITAL ELECTRONICS DESIGN WITH VHDL

(HONORS in ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Design a binary multiplier using VHDL in behavioral model for 4X4 binary multiplier.	L3	CO1	7 M
	b)	Design an adder of two numbers using VHDL.	L3	CO2	7 M
OR					
2	a)	Explain the following with declaration format and an example each. (i) Variable (ii) signal (iii) constant	L2	CO1	7 M
	b)	Discuss about predefined unconstrained arrays. Explain each with an example.	L2	CO2	7 M

UNIT-II					
3	a)	Using process statement write VHDL code for 8X1 multiplexer.	L2	CO3	7 M
	b)	Explain the terms entity and architecture.	L2	CO3	7 M
OR					
4	a)	Design 8 to 3 encoder and model using VHDL.	L3	CO3	7 M
	b)	Describe the signal assignment statement with suitable example.	L2	CO3	7 M
UNIT-III					
5	a)	Model mean calculator for four integers using VHDL function.	L3	CO3	7 M
	b)	Using VHDL procedure model full adder sum and carry.	L3	CO3	7 M
OR					
6	a)	Using VHDL function write a code binary to integer converter.	L2	CO3	7 M
	b)	Using VHDL packages write a code for area of circle.	L2	CO3	7 M
UNIT-IV					
7	a)	Model using VHDL code for a bit odd sequence counter if control input X=0 and even sequence counter if control input X=1.	L3	CO3	7 M
	b)	Explain state machine with suitable example.	L2	CO3	7 M
OR					

8	a)	Design a Decade synchronous counter and model using behavioural VHDL modelling.	L3	CO3	7 M
	b)	Model D Flip-flop using behavioural VHDL modelling.	L3	CO3	7 M
UNIT-V					
9	a)	With a neat sketch explain FPGA Xilinx 4000 series logic cell.	L2	CO4	7 M
	b)	Design 2:1 multiplexer using PLA.	L3	CO4	7 M
OR					
10	a)	(i)Explain FPGA principle and architecture. (ii) Explain one-hot state assignment.	L2	CO4	7 M
	b)	Design and model half adder using FPGA.	L3	CO4	7 M